## **CLAIMS**

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## What is claimed is:

| 1. | 1. A circuit, comprising:   |  |  |  |
|----|---|--|--|--|
| 2  | a first transistor coupled across a first capacitor included in a series of           |  |  |  |
| 3  | stacked capacitors; and   |  |  |  |
| 4  | a second transistor coupled across a second capacitor included in the series          |  |  |  |
| 5  | stacked capacitors, the first transistor coupled to the second transistor, the first  |  |  |  |
| 6  | capacitor coupled to the second capacitor, wherein the first and second transistors   |  |  |  |
| 7  | are adapted to provide a bleed current to the series of stacked capacitors to         |  |  |  |
| 8  | balance a leakage current imbalance in the series of stacked capacitors.              |  |  |  |
|    |   |  |  |  |
| 1  | 2. The circuit of claim 1 further comprising a resistor divider network               |  |  |  |
| 2  | coupled to respective control terminals of the first and second transistors to define |  |  |  |
| 3  | an input reference for the circuit.   |  |  |  |
|    |   |  |  |  |
| 1  | 3. The circuit of claim 2 wherein the resistor divider network                        |  |  |  |
| 2  | comprises at least two resistors coupled to the respective control terminals of the   |  |  |  |
| 3  | first and second transistors.   |  |  |  |
|    |   |  |  |  |
| 1  | 4. The circuit of claim 1 wherein the first and second transistors are                |  |  |  |

coupled to a connection point between the first and second capacitors of the series

- 3 of stacked capacitors, the first and second transistors adapted to maintain a
- 4 voltage at the connection point within an input reference range.
- The circuit of claim 1 wherein the bleed current is substantially equal to the leakage current imbalance in the series of stacked capacitors.
- 1 6. The circuit of claim 1 wherein the bleed current is substantially
  2 equal to zero when a voltage at the connection point remains fixed at a voltage
  3 within an input reference range.
- 7. The circuit of claim 1 wherein the first and second transistors are coupled in a sink-source follower circuit configuration.
- 1 8. The circuit of claim 7 wherein the sink-source follower circuit is 2 coupled to receive an input reference that is a fraction of a voltage applied across 3 the series of stacked capacitors.
- 9. The circuit of claim 8 wherein the input reference is a range of voltages including upper and lower reference voltages, each of which is offset from the fraction of the voltage applied across the series of stacked capacitors.

| 1   | 10.  | The circuit of claim 9 wherein the offset of the upper and lower |                                  |  |
|-----|--|--|----------------------------------|--|
| 2   | reference voltages from the fraction of the voltage applied across the series of       |  |                                  |  |
| 3   | stacked capacitors is zero.  |  |                                  |  |
|     |  |  |                                  |  |
| 1   | 11.  | The circuit of claim 7 wherein the f                             | irst and second transistors      |  |
| 2   | comprise bip   | olar junction transistors.                                       |                                  |  |
|     |  |  |                                  |  |
| 1   | 12.  | The circuit of claim 11 wherein the                              | first and second transistors     |  |
| 2   | comprise a P   | NP transistor and an NPN transistor.                             |                                  |  |
|     |  | *  |                                  |  |
| 1   | 13.  | The circuit of claim 12 further com                              | prising a first resistor coupled |  |
| 2   | to a collector   | of the first transistor to limit the blee                        | d current through the first      |  |
| 3   | transistor, the circuit further comprising a second resistor coupled to a collector of |  |                                  |  |
| 4   | the second transistor to limit the bleed current through the second transistor.        |  |                                  |  |
|     |  |  |                                  |  |
| 1   | 14.  | The circuit of claim 1 wherein the                               | circuit is an active circuit     |  |
| 2   | included in a  | power supply circuit.  |                                  |  |
| • . |  |  |                                  |  |
| 1   | 15.  | A method, comprising:  |                                  |  |
| _   |  |  | encistor to a connection point   |  |
| 2   | providing a bleed current through a first transistor to a connection point             |  |                                  |  |
| .3  | between first and second capacitors included in a series of stacked capacitors if a    |  |                                  |  |
| 4   | voltage at the   | connection point rises above an upp                              | er reference voltage; and        |  |

- 5 providing the bleed current through a second transistor to the connection
- 6 point if the voltage at the connection point falls below a lower reference voltage.
- 1 16. The method of claim 15 wherein the voltage at the connection
- 2 point rises above the upper reference voltage as a result of a leakage current
- 3. imbalance in the series of stacked capacitors, the method further comprising
- 4 balancing the leakage current imbalance with the bleed current.
- 1 17. The method of claim 16 wherein the bleed current is substantially
  - 2 equal to a difference in leakage currents between the first and second capacitors.
  - 1 18. The method of claim 15 wherein the voltage at the connection
  - 2 point falls below the upper reference voltage as a result of a leakage current
  - 3 imbalance in the series of stacked capacitors, the method further comprising
  - 4 balancing the leakage current imbalance with the bleed current.
  - 1 19. The method of claim 18 wherein the bleed current is substantially
  - 2 equal to a difference in leakage currents between the first and second capacitors.
  - 1 20. The method of claim 15 further comprising maintaining the voltage
  - 2 at the connection point within an input reference voltage range defined by the
  - 3 upper and lower reference voltages.

- 1 21. The method of claim 20 wherein an offset between the upper and 2 lower reference voltages is substantially zero.
- 1 22. The method of claim 15 further comprising smoothing an output 2 voltage of a diode bridge of a power supply with the series of stacked capacitors.
- 1 23. The method of claim 15 further comprising switching off the first 2 and second transistors if the voltage at the connection point is between the upper 3 and lower reference voltages.
- 24. A circuit, comprising:

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- a series of stacked capacitors including first and second capacitors coupled
   across a power supply input;
- a first transistor coupled across the first capacitor, the first transistor

  having a control terminal coupled to receive a first reference voltage; and
- 7 transistor have a control terminal coupled to receive a second reference voltage;

a second transistor coupled across the second capacitor, the second

- 8 the first and second capacitors coupled to the series of stacked capacitors at a
- 9 connection point between the first and second capacitors, the first and second
- transistors adapted to provide a bleed current to balance a leakage current
- imbalance in the series of stacked capacitors.

| 1        | 23. The effective   | of claim 24 further comprising.                                |  |
|----------|---|--|--|
| 2        | a first resistor coupled to the first transistor to limit the bleed current           |  |  |
| <b>3</b> | through the first transistor; and   |  |  |
| 4        | a second resistor coupled to the second transistor to limit the bleed current         |  |  |
| 5        | through the second transistor.  |  |  |
|          |   |  |  |
| 1        | 26. The circuit   | of claim 24 further comprising a resistor network              |  |
| - 2      | coupled to the first and second transistors to provide the first and second reference |  |  |
| 3 .      | voltages.   |  |  |
|          |   |  |  |
| 1        | 27. The circuit   | The circuit of claim 26 wherein the first and second reference |  |
| 2        | voltages provided by the resistor network are different from one another.             |  |  |
|          |   |  |  |
| 1        | 28. The circuit   | of claim 26 wherein the first and second reference             |  |

voltages provided by the resistor network are the same.